Christof Schlaak

PhD Student

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cschlaak

I am a second year PhD Student in Computer Science at the Institute for Computing Systems Architecture at the University of Edinburgh on the topic *'High-Level Synthesis of Neural Networks for FPGAs with LIFT'*. Microsoft Research has awarded me a PhD scholarship to carry out my studies. My research interests are centred around hardware design and neural networks. In my research, I want to compile neural network applications to an optimised hardware implementation. I am a member of the LIFT team (lift-project.org) and extend LIFT's high-level functional language and its optimised compilation to include the ability to target FPGAs.
Before my PhD studies, I completed my bachelor and master studies in computer science and worked as a researcher for two years.

Education

since 2018 **PhD Studies**, *University of Edinburgh*, Edinburgh, Scotland, United Kingdom.
In my PhD studies, the goal is to automatically generate optimised FPGA hardware designs specialised for neural network applications. Starting from a hardware-agnostic description in the high-level functional data parallel language Lift, these applications are then compiled to platform-specific VHDL code. In this process, rewrite rules span a vast design space and machine learning techniques as well as performance models help to explore it in order to find an implementation that meets the requirements for e.g. energy-efficiency.

2014–2016 **Master of Science in Computer Science**, *University of Oldenburg*, Oldenburg, Germany.
My master studies had a focus on embedded systems, covering the following subjects: System level design for embedded systems (with SystemC), low energy system design, and testing technologies for embedded systems. I designed hardware in VHDL for FPGAs in a practical training and employed FPGAs in my master's thesis. Translated title of the master's thesis: 'Measurement based execution time and power analyses of synchronous dataflow graphs on FPGA based MPSoCs'. Another class taught me about fuzzy control and artificial neural networks. I developed a wearable computer based on Arduinos and an android app connected via bluetooth.

2011–2014 **Bachelor of Science in Computer Science**, *University of Oldenburg*, Oldenburg, Germany.
Besides covering the basics of computer science, my bachelor studies were specialised on Embedded Systems and Microrobotics (ESMR) with courses about embedded systems, real-time operating systems, HW/SW system design, digital signal and image processing, electrical engineering, control engineering, microrobotics, and microsystems engineering. Translated title of the bachelor's thesis: 'Code generator for automatically configuring an execution time analysis framework for digital signal processing applications'.

Experience

2019–2020 **Teaching Assistant**, *University of Edinburgh*, Edinburgh, Scotland, United Kingdom.
In the course 'Compiling Techinques', I supported students develop their C compilers.

2016–2018 **Researcher**, *OFFIS – Institute for Information Technology*, Oldenburg, Germany.
Full-time work at OFFIS in the department Transportation, in the group Safety & Security Oriented Design Methods & Processes. I contributed to several international projects about (intelligent strategies for) testing and simulation with use-cases mainly from the automotive domain. By designing simulation architectures and developing prototypes for the research projects, I improved my skills in C/C++, python, MATLAB/Simulink and many other tools. Furthermore, I gained experience in project management related tasks (e.g. organising meetings) and in working together in a team.

2011–2016 **Tutor**, *University of Oldenburg*, Oldenburg, Germany.
During my studies at the university I also worked as a tutor, teaching other students (one course per semester) in imperative and object-oriented programming with Java.

Awards

2017 **Excellent Graduation Work**, *University of Oldenburg*, Oldenburg, Germany.
My master's thesis from 2016 was awarded 'Excellent Graduation Work'.

2014 **Federal State Scholarship**, *University of Oldenburg*, Oldenburg, Germany.
I received a Federal State Scholarship in Lower Saxony for outstanding achievements in my bachelor studies.

Talks

Dec 2019 **High-level Synthesis of Neural Networks for FPGAs with Lift** (Poster), *Google's 7th Compiler and Programming Language Summit 2019*, Munich, Germany.

Sep 2019 **Synthesising Neural Networks on FPGAs with Lift** (Talk), *Facebook AI Systems Faculty Summit 2019*, Facebook HQ, Menlo Park, CA, United States.

Jul 2019 **High-level Synthesis of Neural Networks for FPGAs with Lift** (Poster), *Fifteenth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES 2019)*, Fiuggi, Italy.

Apr 2019 **High-level Synthesis of Neural Networks for FPGAs with Lift** (Lightning Talk and Poster), *HiPEAC Computer Systems Week (CSW) Spring 2019*, Edinburgh, United Kingdom.

Publications

2019 B. Bauer, J.S. Becker, T. Peikenkamp, **C. Schlaak** and I. Stierand, *'Design Validation for Embedded Multi-core Systems in the Context of ISO 26262'*, in Workshop on Software Engineering for Applied Embedded RealTime Systems (SEERTS).

2017 **C. Schlaak**, M. Fakih and R. Stemmer, *'Power and Execution Time Measurement Methodology for SDF Applications on FPGA-based MPSoCs'*, in Conference on High Performance and Embedded Architecture and Compilation 2017 (HiPEAC17).